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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/817,270	03/27/2001	Ryoichi Inanami	03180.0278	7690

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EXAMINER	
JOHNSTON, PHILLIP A	

ART UNIT	PAPER NUMBER
2881	

DATE MAILED: 12/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/817,270	INANAMI ET AL.4	
	Examiner	Art Unit	
	Phillip A Johnston	2881	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This Office Action is submitted in response to RCE / Amendment filed 10-07-2004, wherein claims 1,7, and 15 have been amended. Claims 1-21 are pending.

Claims Rejection – 35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

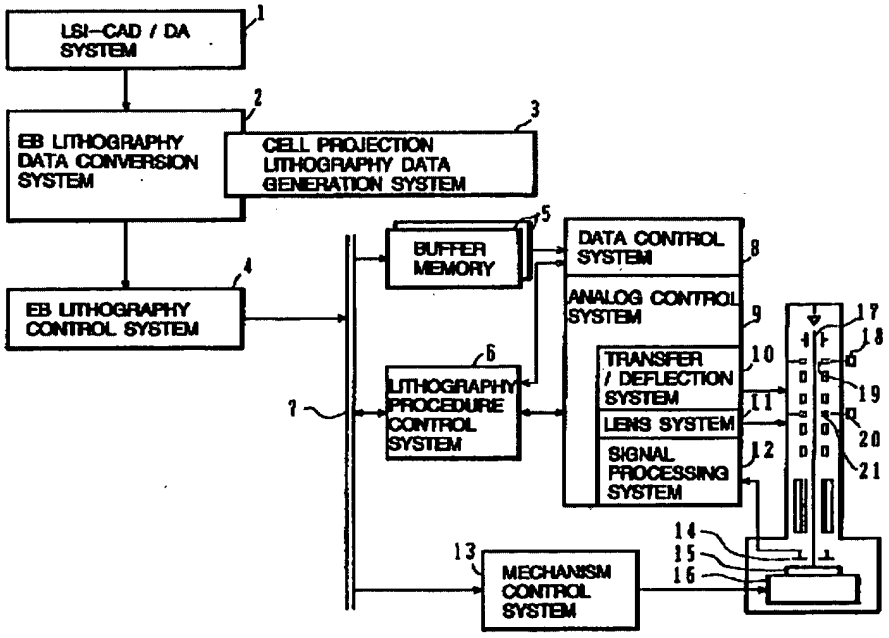
3. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,371,373 to Shibata, in view of Shimada, U.S. Patent No. 5,348,902.

Shibata (373) discloses the following;

(a) A cell projection lithography apparatus and technique including; an LSI device pattern supplied from the LSI CAD/DA system 1 to the electron beam (EB) lithography data conversion system 2 as input data to the EB lithography apparatus. If the input data represents a repeated pattern (which is also called a cell in some LSI-CAD systems) as, for example, patterns of a memory device, then a cell projection lithography technique is utilized to perform efficient writing or delineating operation. The lithography data generated by the data conversion system 2 and the data

generation system 3 is transferred to an EB lithography control system 4 and registered therein. Further, the repeated pattern processed by the EB lithography data generation system 3 of the cell projection lithography is generated as a second transfer mask 21 and installed in a second transfer mask mechanism 20. Further, in order to convert the shot patterns into a beam, the shot patterns are controlled and calibrated through a transfer/deflection system 10 and a lens system 11 in an analog control system 9 and then irradiated as a beam 17 onto an object 15 to be delineated, as recited in claims 1-3,7,9,10, and 15. Figure 3 below and Column 4, line 24-66;

FIG.3

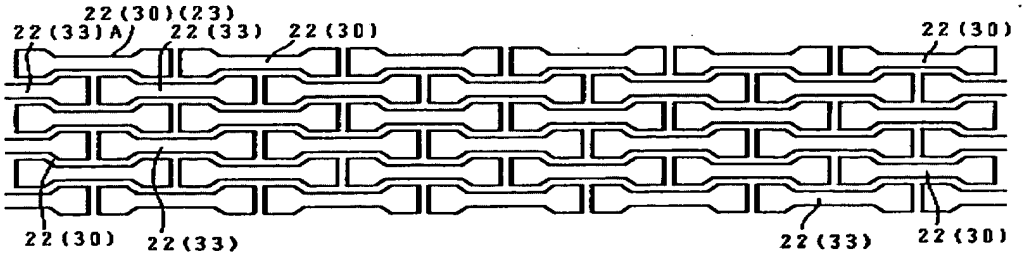


(b) After the lithography data for delineating and the second transfer mask 21 are generated in this way, the EB lithography control system 4 transfers the lithography

data through a system bus 7 to a buffer memory 5 at a high speed. The buffer memory 5 is usually formed of two memory units so that while one of the memory units is receiving the lithography data through the system bus 7, the other of the memory units is transferring the lithography data to a data control system 8 at a high speed for the body of the apparatus in its delineating operation. When the lithography data is the cell projection data, a mask to be used is merely designated and the second transfer mask mechanism 20 is controlled, by using the designated mask to thereby perform the delineating operation, as recited in Claims 13-15. See Column 4, line 44-61;

(c) FIG. 4 shows an example of repeated patterns seen in a memory device or the like. A repetitive unit pattern 22, as shown in FIG. 7, has a repetitive structure 30 (pattern 22 (30) shown in FIG. 4) with respect to an array reference point 23 serving as a start point (pattern 22(30)(23) in FIG. 4). Similarly, the repetitive unit pattern 22 has a repetitive structure 33 with respect to an array reference point A (pattern 22(33)A in FIG. 4). See Figure 4 below; and Column 5, line 18-25;

FIG.4

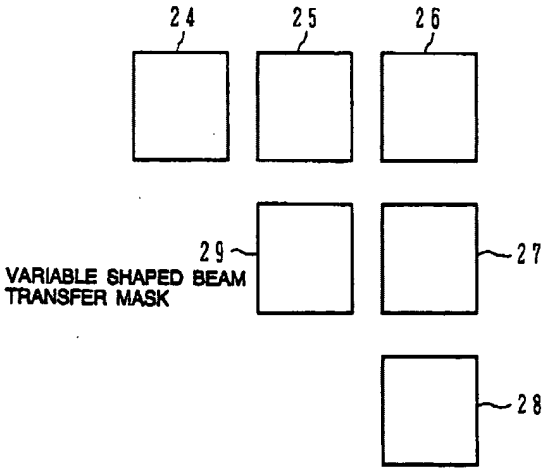


(d) In this method, noting the repeatability of devices, a cell as the repetitive pattern unit is used as a transfer mask and the transfer mask is used also as a

variable shaped beam transfer mask, thereby reducing the shot number remarkably and increase a lithography throughput, as recited in claims 6 and 15. See Column 1, line 33-40;

(e) If the beam 17 is a variable shaped beam, the beam 17 is subjected to shaping operations by a first transfer mask 19 of the variable shaped beam installed in a first transfer mask mechanism 18 and by a mask (a mask 29 in FIG. 6) of the variable shaped beam in the second transfer masks 21 disposed in the second transfer mask mechanism 20.FIG. 6 shows an example of a layout of the second transfer masks 21 used in the cell projection lithography. The masks 24 to 28 are for the cell projection lithography, while the mask 29 is for the variable shaped beam method, as recited in claims 2,5,8, and 16. See Column 5, line 50-54.

FIG.6



Shibata (373) as applied above fails to teach;

(a) The use of a standard cell library where cells having functions, shapes of outlines, and input/output positions are recorded, as recited in claims 1,4,7,12,13,15 and 20;

(b) Conducting logic synthesis, as recited in claims 7,9,10,15, and 18; and

(c) Placement and routing, as recited in claims 1,7,11,14,19, and 21.

However, Shimada (902) discloses the following;

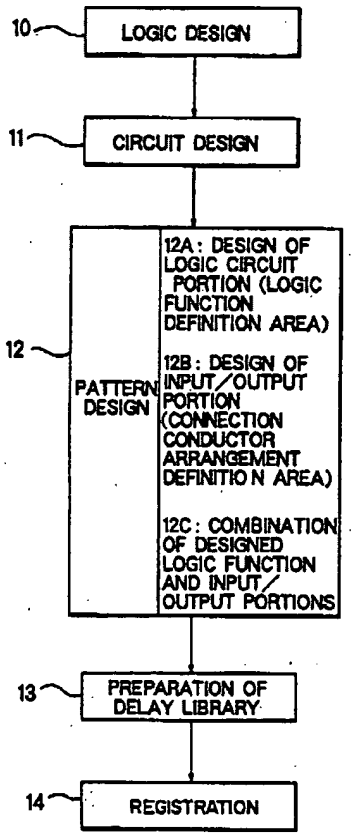
(a) In an automatic placing and routing system for fabricating a semiconductor integrated circuit device (hereinafter sometimes referred to simply as "LSI device"), cells are placed and routed between terminals on a semiconductor substrate. The cells include basic cells of a standard cell system or a cell-based system, and are registered in a library as a functional block of, for example, a flip-flop or a two-input NAND gate. The layout of these cells is prepared through an automatic cell layout preparation program on the basis of a circuit diagram designed in advance. This automatic cell layout preparation program is for generating an actual cell pattern on the basis of circuit diagram information, a layout rule on the fabrication process of the LSI device and performance designating information such as the width and length (W/L) of the transistor (shape).

Design automation (DA) systems for automatic placing and routing of basic cells include those marketed by various computer-aided design (CAD) system makers and those internally fabricated by semiconductor integrated circuit device makers.

Individual DA systems, however, are required to meet the input/output terminal requirements specific thereto.

FIG. 2, shows the steps for producing a library of basic cells include logic designing 10, circuit designing 11, pattern designing 12, production of a delay library 13, and registration 14 of the data obtained in the foregoing steps. In the logic designing step 10 (logic synthesis), the kind of gate function to be developed for a cell is studied, and the logics designed to realize the particular function, as recited in claims 1,4,7,9,12-15, and 17-21. See Figure 2 below; and Column 1, line 14-60.

FIG. 2



(b) A cell with a pattern designed by the above-mentioned method is regarded as a basic cell of a standard cell system of a semiconductor integrated circuit and is registered in the library. A multiplicity of cells registered in the library are placed and routed in order to constitute a semiconductor integrated circuit device as required, and mask patterns are formed from information thus obtained. These masks are used for forming a semiconductor integrated circuit device on a semiconductor substrate.

A library entered with cells having a pattern designed by the above-mentioned method is applied to the automatic placing and routing by a predetermined DA system, whereby the data for forming a mask pattern of an intended semiconductor integrated circuit device is formed. On the basis of this data, a predetermined mask pattern is specified, and by utilizing a photomask or an electron beam plotter according to this pattern, a desired semiconductor integrated circuit device is fabricated on the wafer through the well-known various wafer processes, as recited in claims 1,7,11,14,19, and 21.

Therefore, it would have been obvious to one of ordinary skill in the art, that the LSI/CAD data of Shibata's (373) lithography exposure system can be modified to use the standard cell library data of Shimada (902), making it possible to select the repetitive standard cells to be included on the mask.

Conclusion

6. Any inquiry concerning this communication or earlier communications should be

directed to Phillip Johnston whose telephone number is (571) 272-2475. The examiner can normally be reached on Monday-Friday from 7:30 am to 4:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiners supervisor John Lee can be reached at (571) 272-2477. The fax phone number for the organization where the application or proceeding is assigned is 703 872 9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PJ

December 20, 2004

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